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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,539	03/23/2004	Lee D. Whetsel	TI-25300.2	2498

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EXAMINER	
RADOSEVICH, STEVEN D	
ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 09/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,539	WHETSEL, LEE D.	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *1-34* is/are withdrawn from consideration.

5)☒ Claim(s) 37 is/are allowed.

6)☒ Claim(s) *35 and 38-42* is/are rejected.

7)☒ Claim(s) *36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-42 are present for examination. Acknowledgment is made that claims 1-34 have been canceled by the applicant in response to the correspondence from the USPTO mailed to the applicant on 02/24/2006, and as such claims 1-34 are not being given further consideration within this examination.

Priority

Acknowledgement is made that the **NEW claims** 35-42 are claiming priority back to the date 03/27/1997 used in the previous examination of the instant application.

Drawings

The drawings are not objected to at this time since it does not appear that at this time there are any issues with the drawings in view of the **NEW claims** 35-42 of the instant application. Applicant is reminded that the instant applicant previously rejected for double patenting issues in view of US patent 6199182 should as per 37 CFR § 1.83 (b) When the invention consists of improvement on an old machine the drawing must when possible exhibit, in one or more views, the improved portion itself, disconnected from the old structure, and also in another view, so much only of the old structure as will suffice to show the correction of the invention therewith.

Claim Objections

Claim 36 is objected to because of the following informalities:

In lines 2-3 of the claim it reads, "a multiplexer, which has having an output" wherein it should read, "a multiplexer, which has an output" such that the claim language makes sense.

Appropriate correction is required.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 35 and 38-42 are rejected on the ground of nonstatutory double patenting over claim 4 of U. S. Patent No. 6199182 B1 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

1. As per claim 35 of the instant applicant, an integrated circuit comprising:

   a. A substrate of semiconductor material (6199182: semiconductor body);

   b. Pads formed on the semiconductor material (6199182: terminal pad);

c. Functional circuits formed on the substrate and having functional output leads coupled to the pads (6199182: at least one integrated circuit formed at the surface thereof);

d. Output buffer circuitry formed on the substrate, for each functional output lead, the buffer circuitry having a buffer input lead connected to the functional output lead and having a buffer output lead connected to a pad (6199182: output buffer);

e. Test access port circuitry formed on the substrate, the test access port circuitry having a test data input lead, a test data output lead, a test clock input lead, and a test mode select input lead, all connected to the pads (6199182: control circuitry);

f. Scan cells formed on the substrate and connected to the test access port circuitry, to the test data input lead, and to the test data output lead (6199182: terminal buffer);

g. Test leads formed on the substrate and connected to the pads (signal path); and

h. Scannable switch circuitry formed on the substrate and connected to the test access port circuitry, to the test data input lead, and to the test data output lead, the scannable switch circuitry selectively connecting a buffer input lead and a buffer output lead to the test leads (6199182: first and second test switches).

The instant application and the US Patent share the same common circuitry that performs the same function(s), which render the instant application in conflict with the

US Patent, wherein each limitation within the instant application is directly concurrent with the limitations within the US Patent as per claim 4 as has been shown above.

2. As per claim 38 within the instant application, the integrated circuit in which the test leads are input leads and output leads is an obvious sign choice since the leads connect the input and output of the circuitry formed on the semiconductor material to the pads formed in the semiconductor material which allow connectivity of the semiconductor and all the functional circuitry there upon to external device(s) providing and receiving data.

3. As per claim 39 within the instant applicant, the integrated circuit in which a scan cell selectively connects a functional output lead to the buffer input lead is an obvious connections design choice since a scan cell of a scan chain receives the test data output from the functional logic core as is well known and the output buffer is connected to the terminal pad, the test data output must traverse through the buffer to reach the pad and any other external device trying to receive the test data.

4. As per claim 40 within the instant application, the integrated circuit including a bus hold circuit connected to the buffer output lead is an obvious design choice such that the test data can be held within the semiconductor until an external device is ready receive, or connected to the specific pad to receive the data held within.

5. As per claim 41 within the instant application, the integrated circuit including an electrostatic discharge circuit connected to the buffer output lead is an obvious design choice such that the buffer can be reset/discharged fully after use so as not to allow residual and potentially damaging charge to remain within the buffer.

6. As per claim 42 within the instant application, the integrated circuit including a bus hold circuit and an electrostatic discharge circuit connected to the buffer output lead is an obvious sign choice wherein as described above the discharge circuit will protect the buffer from potentially damaging residual charge while holding the charge/date within the hold bus which is designed to hold charge/date until as also described above external device is ready receive, or is connected to receive the charge/data held within.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GUY LAMARRE
PRIMARY EXAMINER

Steven D. Radosevich
Examiner
Art Unit 2138